

FM25e64

64Kb Serial Low Energy F-RAM Memory



FEATURES

64K bit Ferroelectric Nonvolatile RAM

- Organized as 8,192 x 8 bits
- High Endurance 1 Trillion (10¹²) Read/Writes
- 36 Year Data Retention at +75°C
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Fast SPI Interface

- Up to 20 MHz Frequency
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)
- Software Write-Protection (BP bits)
- Hardware Write-Protect (/WP pin)

Active-Low RESET Input

- Holds Device in Reset State While Power Supply Stabilizes
- Reduces Time to First F-RAM Access
- Allows Freedom of Power Supply Ramp Rates

Low Voltage/ Low Energy Consumption

- VDD = 1.8V ±0.1V (-1 version)
- VDD = 1.5V +0.15V, -0.1V (-2 version)
- 20 µA (typ.) Active Current at 1 MHz
- 0.1 µA (typ.) Standby Current

Industry Standard Configuration

- Industrial Temperature -40°C to +85°C
- 8-pin “Green”/RoHS SOIC Package

DESCRIPTION

The FM25e64 is a low voltage, low energy 64-kilobit nonvolatile memory employing an advanced F-RAM process. It provides reliable data retention for 36 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

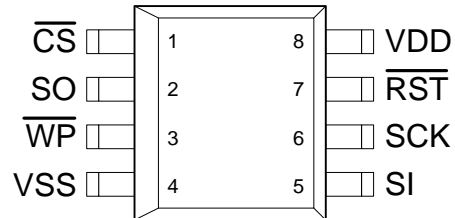
The FM25e64 performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte has been successfully transferred to the device. The next bus cycle may commence immediately without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. The FM25e64 is capable of supporting 10¹² read/write cycles, or a million times more write cycles than EEPROM.

These capabilities make the FM25e64 ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss.

The FM25e64 provides substantial benefits to users of serial EEPROM as a hardware drop-in replacement. The FM25e64 uses the high-speed SPI

bus, which enhances the high-speed write capability of F-RAM technology. Device specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

PIN CONFIGURATION



Pin Name	Function
/CS	Chip Select
SCK	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
/RST	Reset Input
/WP	Write Protect Input
VDD	Supply Voltage
VSS	Ground

This is a product that has fixed target specifications but are subject to change pending characterization results.

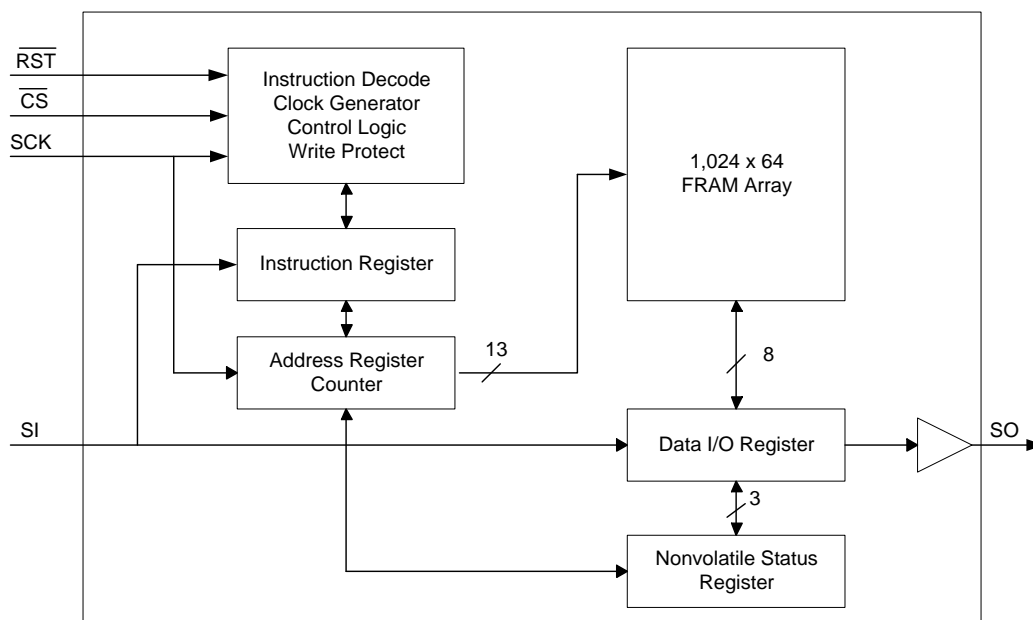


Figure 1. Block Diagram

PIN DESCRIPTIONS

Pin Name	I/O	Description
/RST	Input	Reset Input: This active-low pin is used to hold the memory in a reset state while power is being stabilized. When /RST is low, the interface is inactive and the SPI state machine is reset. Once Vdd is within spec, the /RST pin may be driven high. The memory is ready for commands within t _{PU} .
/CS	Input	Chip Select: This active low input activates the device. When high, the device enters low-power standby mode and ignores other inputs. When low, the device internally activates the SCK signal. A falling edge on /CS must occur prior to every op-code.
SCK	Input	Serial Clock: All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Since the device is static, the clock frequency may be any value between 0 and 20 MHz and may be interrupted at any time.
SI	Input	Serial Input: All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet I _{DD} specifications.
SO	Output	Serial Output: This is the data output pin. It is driven during a read and remains tri-stated at all other times including when /RST is low. Data transitions are driven on the falling edge of the serial clock.
/WP	Input	Write Protect: This active low pin prevents write operations to the status register only. A complete explanation of write protection is provided on pages 7 and 8.
VDD	Supply	Power Supply
VSS	Supply	Ground

OVERVIEW

The FM25e64 is a low energy serial F-RAM memory. The memory array is logically organized as 8,192 x 8 and is accessed using an industry standard Serial Peripheral Interface or SPI bus. Functional operation of the F-RAM is similar to serial EEPROMs. The major difference between the FM25e64 and a serial EEPROM with the same pinout is the F-RAM's superior write performance.

MEMORY ARCHITECTURE

When accessing the FM25e64, the user addresses 8,192 locations of 8 data bits each. These data bits are shifted serially. The addresses are accessed using the SPI protocol, which includes a chip select, an op-code, and a two-byte address. The upper 3 bits of the address range are 'don't care' values. The complete address of 13-bits specifies each byte address uniquely.

Most functions of the FM25e64 either are controlled by the SPI interface or are handled automatically by on-board circuitry. The access time for memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. So, by the time a new bus transaction can be shifted into the device, a write operation will be complete. This is explained in more detail in the interface section.

Users expect several obvious system benefits from the FM25e64 due to its fast write cycle and high endurance as compared to EEPROM. In applications that have a limited power budget, the fast-write and low-power operation provides a much lower energy solution for nonvolatile store compared to EEPROM since the access is completed quicker and at a very low voltage. By contrast, an EEPROM requires milliseconds to perform a write operation and at much higher currents.

RESET

A reset input (/RST) is provided as a means to hold the memory interface in a reset state during power cycle events. When /RST is driven low, the memory enters a reset condition. In this state, the interface is locked out and the SO pin is high impedance. When /RST is driven high, the memory enters a normal operating mode after the t_{PU} time is satisfied. Driving /RST low during a read or write operation will abort the operation and data may be lost.

Note: The FM25e64 contains no power management circuits. To ensure proper operation, the user is responsible for /RST being held active (low) while V_{DD} voltage stabilizes and is within the specified DC min/max limits. It is recommended that the part is not powered down with chip enable active.

SERIAL PERIPHERAL INTERFACE – SPI BUS

The FM25e64 employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 20 MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25e64 operates in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. A typical system configuration uses one or more FM25e64 devices with a microcontroller that has a dedicated SPI port, as Figure 2 illustrates. Note that the clock, data-in, and data-out pins are common among all devices. The Chip Select pin must be driven separately for each FM25e64 device.

For a microcontroller that has no dedicated SPI bus, a general purpose port may be used. Figure 3 shows a configuration that uses the MCU GPIO pins.

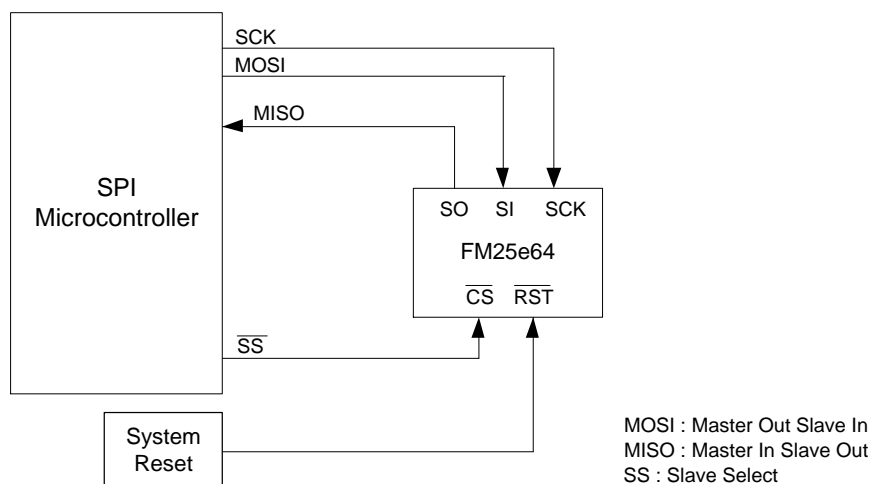


Figure 2. System Configuration with SPI port

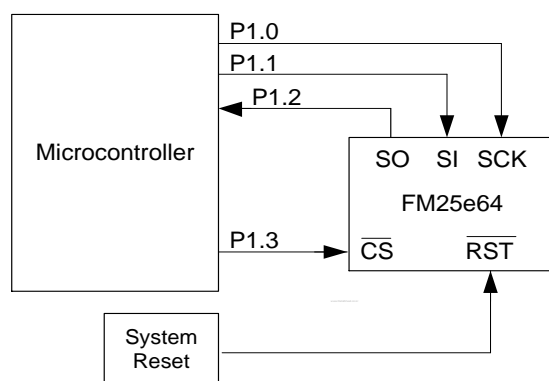


Figure 3. System Configuration without SPI port

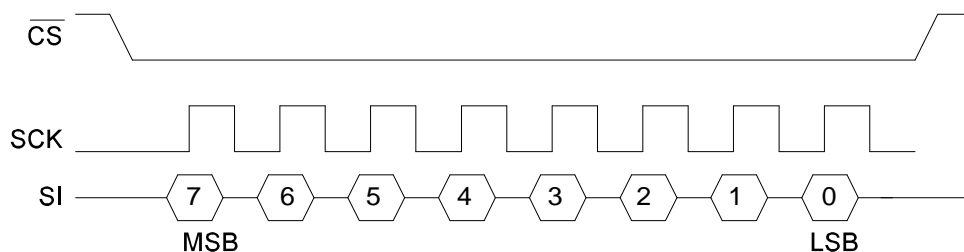
Protocol Overview

The SPI interface is a synchronous serial interface using clock and data pins. Once chip select is activated by the bus master, the FM25e64 will begin monitoring the clock and data lines. The relationship between the falling edge of /CS, the clock and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM25e64 supports Modes 0 and 3. Figure 4 shows the required signal relationships for Modes 0 and 3. For both modes, data is clocked into the FM25e64 on the rising edge of SCK and data is expected on the first rising edge after /CS goes active. If the clock begins from a high state, it will fall prior to beginning data transfer in order to create the first rising edge.

The SPI protocol is controlled by op-codes. These op-codes specify the commands to the device. After /CS is activated the first byte transferred from the bus master is the op-code. Following the op-code, any addresses and data are then transferred. Note that the WREN and WRDI op-codes are commands with no subsequent data transfer.

Important: The /CS pin must go inactive after an operation is complete and before a new op-code can be issued. There is one valid op-code only per active chip select.

SPI Mode 0: CPOL=0, CPHA=0



SPI Mode 3: CPOL=1, CPHA=1

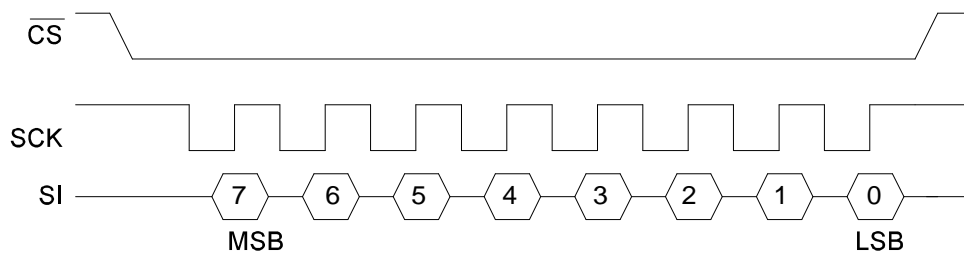


Figure 4. SPI Modes 0 & 3

Power Up to First Access

The FM25e64 is not accessible for a period of time (t_{PU}) after power up. Users must comply with the timing parameter t_{PU} , which is the minimum time from /RST deasserted to the first /CS low.

Data Transfer

All data transfers to and from the FM25e64 occur in 8-bit groups. They are synchronized to the clock signal (SCK), and they transfer most significant bit (MSB) first. Serial inputs are registered on the rising edge of SCK. Outputs are driven from the falling edge of SCK.

Command Structure

There are six commands called op-codes that can be issued by the bus master to the FM25e64. They are listed in the table below. These op-codes control the functions performed by the memory. They can be divided into three categories. First, there are commands that have no subsequent operations. They perform a single function such as to enable a write operation. Second are commands followed by one byte, either in or out. They operate on the Status Register. The third group includes commands for memory transactions followed by address and one or more bytes of data.

Table 1. Op-code Commands

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110b
WRDI	Write Disable	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read Memory Data	0000 0011b
WRITE	Write Memory Data	0000 0010b

WREN – Set Write Enable Latch

The FM25e64 will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the Status Register (WRSR) and writing the memory (WRITE).

Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit – only the WREN op-code can set this bit. The WEL bit will be automatically cleared on the rising edge of /CS following a WRDI, a WRSR, or a WRITE operation. This prevents further writes to the Status Register or the F-RAM array without another WREN command. Figure 5 below illustrates the WREN command bus configuration.

WRDI – Write Disable

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the Status Register and verifying that WEL=0. Figure 6 illustrates the WRDI command bus configuration.

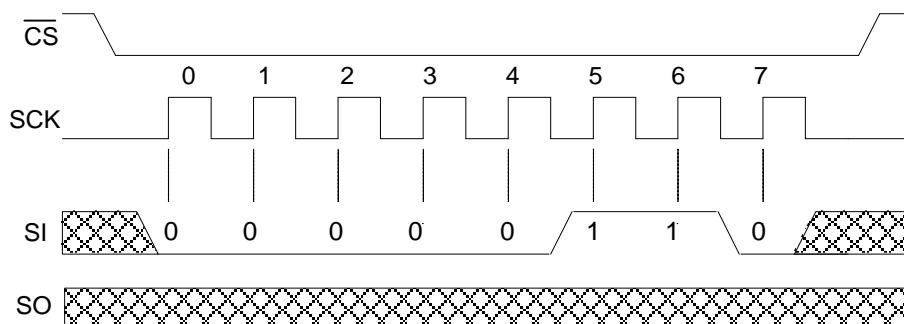


Figure 5. WREN Bus Timing

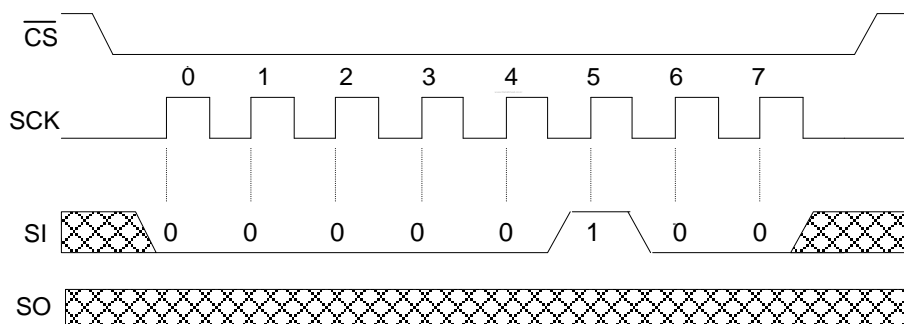


Figure 6. WRDI Bus Timing

RDSR – Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading Status provides information about the current state of the write protection features. Following the RDSR op-code, the FM25e64 will return one byte with the contents of the Status Register. The Status Register is described in detail in a later section.

WRSR – Write Status Register

The WRSR command allows the user to select certain write protection features by writing a byte to the Status Register. Prior to issuing a WRSR command, the /WP pin must be high or inactive. Note that on the FM25e64, /WP only prevents writing to the Status Register, not the memory array. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch.

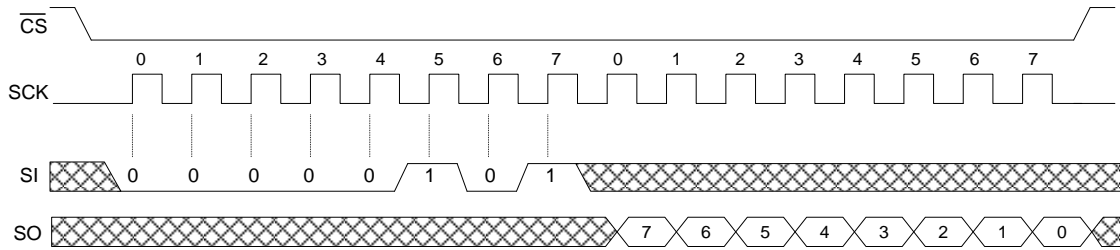


Figure 7. RDSR Bus Timing

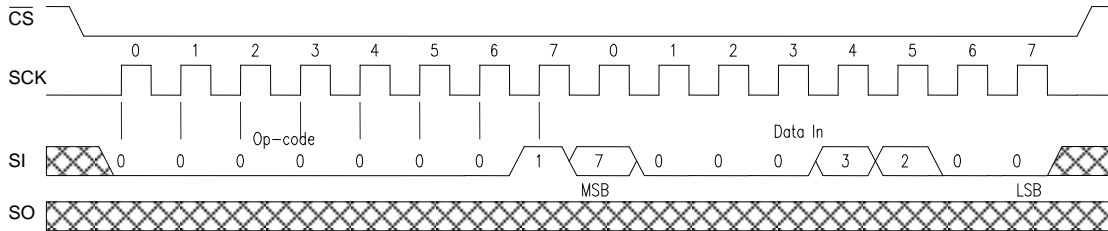


Figure 8. WRSR Bus Timing (WREN not shown)

STATUS REGISTER & WRITE PROTECTION

The write protection features of the FM25e64 are multi-tiered. A WREN op-code must be issued prior to any write operation. Assuming that writes are enabled using WREN, writes to memory are controlled by the Status Register. As described above, writes to the Status Register are performed using the WRSR command and subject to the /WP pin. The Status Register is organized as follows.

Table 2. Status Register

Bit	7	6	5	4	3	2	1	0
Name	WPEN	0	0	0	BP1	BP0	WEL	0

Bits 0 and 4-6 are fixed at 0 and cannot be modified. Note that bit 0 (“Ready” in EEPROMs) is unnecessary as the F-RAM writes in real-time and is never busy. The WPEN, BP1 and BP0 control write protection features. They are nonvolatile (shaded yellow). The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in the following table.

Table 3. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	1800h to 1FFFh (upper ¼)
1	0	1000h to 1FFFh (upper ½)
1	1	0000h to 1FFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The WPEN bit controls the effect of the hardware /WP pin. When WPEN is low, the /WP pin is ignored. When WPEN is high, the /WP pin controls write access to the Status Register. Thus the Status Register is write protected if WPEN=1 and /WP=0.

This scheme provides a write protection mechanism, which can prevent software from writing the memory under any circumstances. This occurs if the BP1 and BP0 are set to 1, the WPEN bit is set to 1, and /WP is set to 0. This occurs because the block protect bits prevent writing memory and the /WP signal in hardware prevents altering the block protect bits (if WPEN is high). Therefore in this condition, hardware must be involved in allowing a write operation. The following table summarizes the write protection conditions.

Table 4. Write Protection

WEL	WPEN	/WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

MEMORY OPERATION

The SPI interface, which is capable of a relatively high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike SPI-bus EEPROMs, the FM25e64 can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory begin with a WREN op-code with /CS being asserted and deasserted. The next op-code is WRITE. The WRITE op-code is followed by a two-byte address value. The upper 3-bits of the address are ignored. In total, the 13-bits specify the address of the first data byte of the write operation. This is the starting address of the first data byte of the write operation. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps /CS low. If the last address of 1FFFh is reached, the counter will roll over to 0000h. Data is written MSB first. The rising edge of /CS terminates a WRITE operation. A write operation is shown in Figure 9.

EEPROMs use page buffers to increase their write throughput. This compensates for the technology’s inherently slow write operations. F-RAM memories do not have page buffers because each byte is written to the F-RAM array immediately after it is clocked in (after the 8th clock). This allows any number of bytes to be written without page buffer delays.

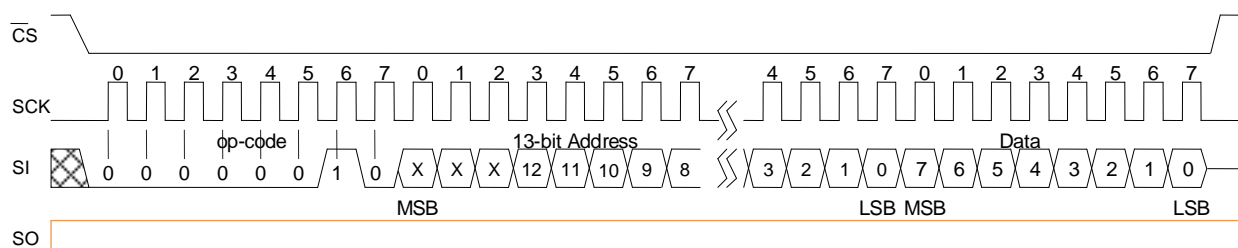


Figure 9. Memory Write (WREN not shown)

Read Operation

After the falling edge of /CS, the bus master can issue a READ op-code. Following the READ command is a two-byte address value. The upper 3-bits of the address are ignored. In total, the 13-bits specify the address of the first byte of the read operation. This is the starting address of the first byte of the read operation. After the op-code and address are issued, the device drives out the read data on the next 8 clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and /CS is low. If the last address of 1FFFh is reached, the counter will roll over to 0000h. Data is read MSB first. The rising edge of /CS terminates a READ operation. A read operation is shown in Figure 10.

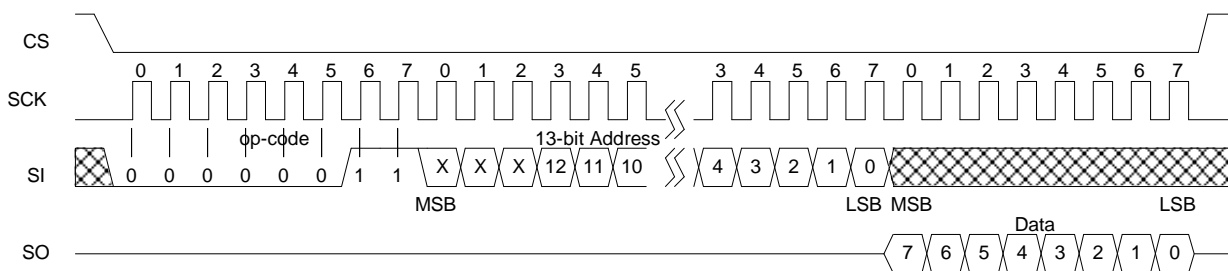


Figure 10. Memory Read

ENDURANCE

The FM25e64 devices are capable of being accessed at least 10^{12} times, reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis for each access (read or write) to the memory array. The F-RAM architecture is based on an array of rows and columns. Rows are defined by A12-A3 and column addresses by A2-A0. See Block Diagram (pg 2) which shows the array as 1K rows of 64-bits each. The entire row is internally accessed once whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation. The table below shows endurance calculations for a system that has a repeating loop to the F-RAM. Suppose that the MCU polls (reads or writes) the F-RAM at a constant repeat rate for the lifetime of the product. The routine accesses the same locations every time the loop is run. This causes each byte to experience one endurance cycle through the loop. F-RAM read and write endurance is virtually unlimited even for loops that repeat at a 1ms rate.

Table 5. Time to Reach Endurance Limit for Repeating Loop

Cycle Time of Repeating Loop	Endurance Cycles/sec.	Endurance Cycles/year	Years to Reach Limit (10^{12})
1 ms	1000	3.15×10^{10}	31.7
5 ms	200	6.30×10^9	158.7
20 ms	50	1.58×10^9	634.9

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +2.4V
V_{IN}	Voltage on any pin with respect to V_{SS}	-1.0V to +2.4V and $V_{IN} < V_{DD} + 0.7V$
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage	
	- Human Body Model (AEC-Q100-002 Rev. E)	TBD
	- Charged Device Model (AEC-Q100-011 Rev. B)	TBD
	- Machine Model (AEC-Q100-003 Rev. E)	TBD
	Package Moisture Sensitivity Level	MSL-1

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply Voltage FM25e64-1 FM25e64-2	1.70 1.40	1.8 1.5	1.90 1.65	V V	
I_{DD1}	VDD Supply Current (FM25e64-1) @ SCK = 1.0 MHz @ SCK = 20.0 MHz		20 400	50 900	μA μA	1
I_{DD2}	VDD Supply Current (FM25e64-2) @ SCK = 1.0 MHz @ SCK = 20.0 MHz		20 300	40 600	μA μA	1
I_{SB}	Standby Current FM25e64-1 FM25e64-2	— - -	0.1 0.1	5 3	μA μA	2
I_{LI}	Input Leakage Current	-		± 1	μA	3
I_{LO}	Output Leakage Current	-		± 1	μA	3
V_{IH}	Input High Voltage	$0.75 V_{DD}$		$V_{DD} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.3		$0.25 V_{DD}$	V	
V_{OH}	Output High Voltage @ $I_{OH} = -1\text{ mA}$	$V_{DD} - 0.3$		-	V	
V_{OL}	Output Low Voltage @ $I_{OL} = 1\text{ mA}$	-		0.2	V	

Notes

- SCK toggling between $V_{DD} - 0.2V$ and V_{SS} , other inputs V_{SS} or $V_{DD} - 0.2V$. SO=open.
- SCK = SI = /CS = V_{DD} . All inputs V_{SS} or V_{DD} .
- $V_{SS} \leq V_{IN} \leq V_{DD}$ and $V_{SS} \leq V_{OUT} \leq V_{DD}$.

AC Parameters ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 30\text{pF}$, unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
f_{CK}	SCK Clock Frequency	0	20	MHz	
t_{CH}	Clock High Time	22		ns	1
t_{CL}	Clock Low Time	22		ns	1
t_{CSU}	Chip Select Setup	10		ns	
t_{CSH}	Chip Select Hold	10		ns	
t_{OD}	Output Disable Time		20	ns	2
t_{ODV}	Output Data Valid Time		20	ns	
t_{OH}	Output Hold Time	0		ns	
t_D	Deselect Time	60		ns	
t_R	Data In Rise Time		50	ns	2,3
t_F	Data In Fall Time		50	ns	2,3
t_{SU}	Data Setup Time	5		ns	
t_H	Data Hold Time	5		ns	

Notes

- $t_{CH} + t_{CL} = 1/f_{CK}$.
- Characterized but not 100% tested in production.
- Rise and fall times measured between 10% and 90% of waveform.

Capacitance ($T_A = 25^\circ\text{C}$, $f=1.0\text{ MHz}$, $V_{DD} = 1.6\text{V}$)

Symbol	Parameter	Min	Max	Units	Notes
C_O	Output Capacitance (SO)	-	8	pF	1
C_I	Input Capacitance	-	6	pF	1

Notes

- This parameter is periodically sampled and not 100% tested.

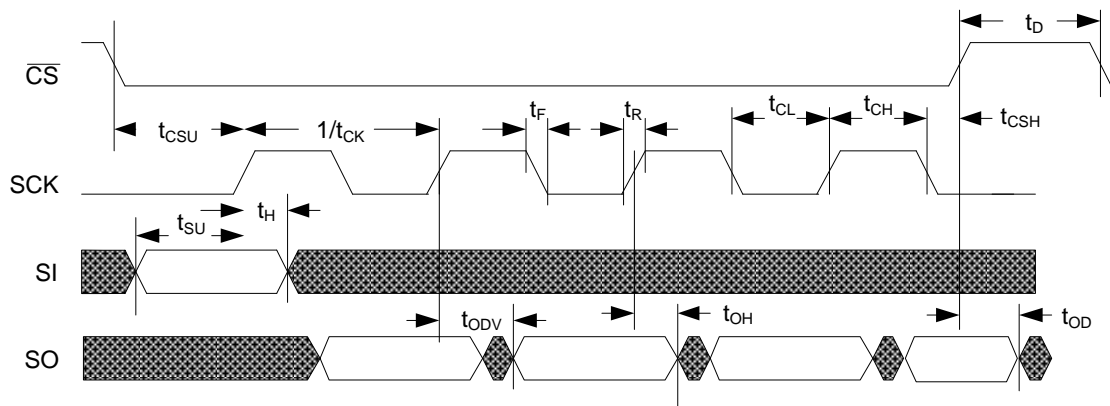
AC Test Conditions

Input Pulse Levels 10% and 90% of V_{DD} —
 Input rise and fall times 5 ns
 Input and output timing levels 0.5 V_{DD}
 Output Load Capacitance 30 pF

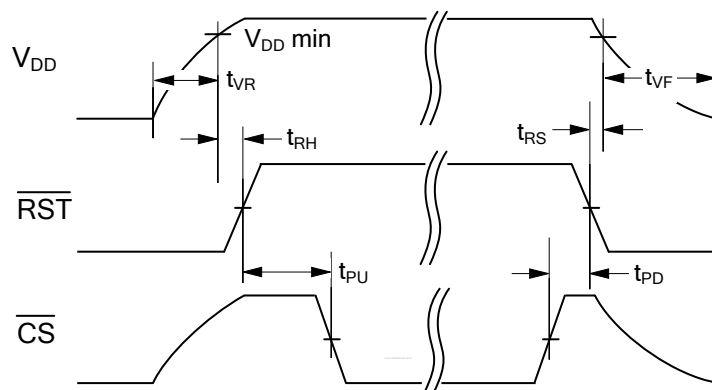
Data Retention

Symbol	Parameter	Min	Max	Units	Notes
T_{DR}	@ $+85^\circ\text{C}$	10	-	Years	
	@ $+80^\circ\text{C}$	18	-	Years	
	@ $+75^\circ\text{C}$	36	-	Years	

Serial Data Bus Timing



Power Cycle Timing



Power Cycle Timing ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise specified)

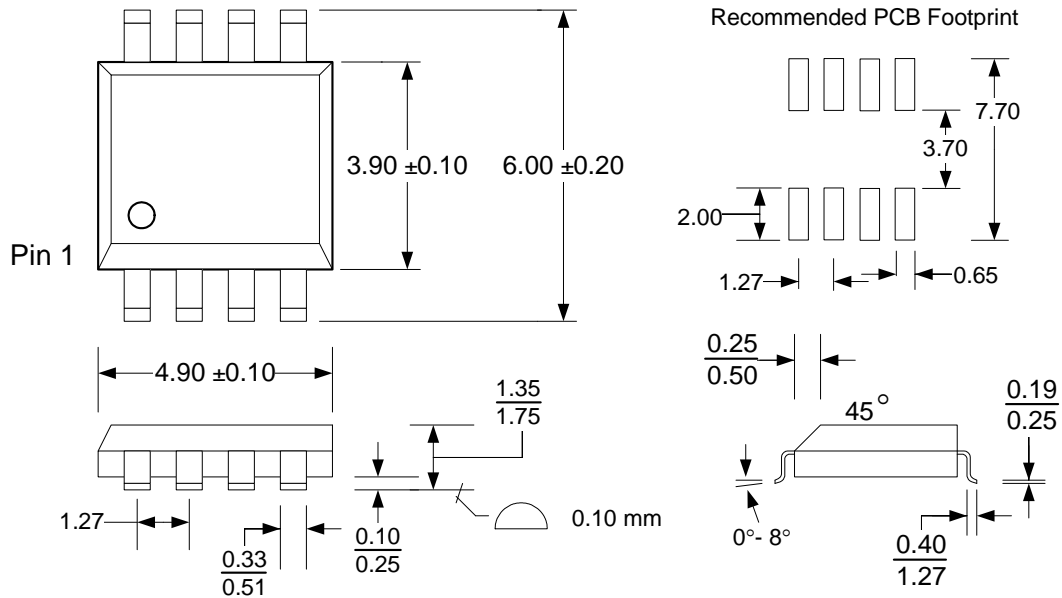
Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	\overline{RST} High to First Access Start	10	-	μs	
t_{PD}	Last Access Complete to $V_{DD}(\text{min})$	0.2	-	μs	
t_{VR}	V_{DD} Rise Time	1	-	$\mu\text{s}/\text{V}$	1
t_{VF}	V_{DD} Fall Time	1	-	$\mu\text{s}/\text{V}$	1
t_{RH}	\overline{RST} Hold Time after $V_{DD}(\text{min})$ at Power Up	0	-	μs	
t_{RS}	\overline{RST} Setup Time to $V_{DD}(\text{min})$ at Power Down	0	-	μs	

Notes

1. This parameter is guaranteed by design.

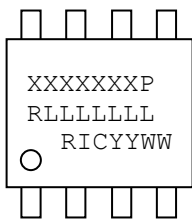
MECHANICAL DRAWING

8-pin SOIC (JEDEC MS-012 variation AA)



Refer to JEDEC MS-012 for complete dimensions and notes.
All dimensions in millimeters.

SOIC Package Marking Scheme



Legend:

XXXXXXX= part number, P= package type (G=SOIC)
R=rev code, LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

Example: FM25E64-1, "Green" SOIC package, Year 2012, Work Week 17

FM25E641G
ESA00002G1
RIC1217

REVISION HISTORY

Revision	Date	Summary
1.0	3/16/2012	Initial Release

ORDERING INFORMATION

Part Number	Operating Voltage	Package
FM25e64-1G	1.8V ($\pm 0.1V$)	"Green" 8-pin SOIC
FM25e64-1GTR	1.8V ($\pm 0.1V$)	"Green" 8-pin SOIC, Tape & Reel
FM25e64-2G	1.5V (+0.15V, -0.1V)	"Green" 8-pin SOIC
FM25e64-2GTR	1.5V (+0.15V, -0.1V)	"Green" 8-pin SOIC, Tape & Reel